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For

LOW RC STRUCTURES FOR ROUTING BODY-BIAS VOLTAGE

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LOW RC STRUCTURES FOR ROUTING BODY-BIAS VOLTAGE

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

5 The present invention generally relates to semiconductor chips and MOSFETS (metal oxide semiconductor field effect transistors). More particularly, the present invention relates to the field of routing body-bias voltage to the MOSFETS using a structure having a low RC.

10 RELATED ART

 Generation of the physical layout of a semiconductor device having MOSFETS (metal oxide semiconductor field effect transistors) formed on a semiconductor substrate is a challenging task. An extensive amount of time and resources are spent during the creation of the physical layout. However, consumption of resources can be
15 minimized if new physical layouts utilize substantial portions of existing physical layouts. For example, a new physical layout having MOSFETS that are body-biased would be less expensive to generate if an existing physical layout having MOSFETS without body-bias is utilized and modified according to the needs of the new physical design. Unfortunately, this process of modifying the existing physical layout typically
20 requires forming an additional routing layer for the body-bias voltage on the surface of the semiconductor device, creating a serious issue since the existing physical layout utilizes most, if not all, available surface area.

SUMMARY OF THE INVENTION

Low RC structures for routing body-bias voltage are provided and described. These low RC structures are comprised of a deep well structure coupled to a metal structure.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the present invention.

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Figure 1 illustrates a top view of a pFET formed in an N-well in accordance with an embodiment of the present invention, showing the pFET having a body-bias voltage V_{nw} applied to its bulk/body B terminal.

10 Figure 2A illustrates the relative positioning of an N-well and a deep N-well region beneath a surface of a semiconductor device in accordance with an embodiment of the present invention.

15 Figure 2B illustrates a side view of a deep N-well region coupled to the N-well_1 and the N-well_2 in accordance with an embodiment of the present invention, showing the routing of the body-bias voltage.

20 Figure 3A illustrates a top view of a first arrangement of the N-well_1 and the N-well_2 in accordance with an embodiment of the present invention.

Figure 3B illustrates a top view of a second arrangement of the N-well_1 and the N-well_2 in accordance with an embodiment of the present invention.

Figure 4 illustrates a top view of a semiconductor device in accordance with an embodiment of the present invention, showing multiple areas each area corresponding to a separate layout pattern for the deep N-well.

5 Figure 5A illustrates a top view of multiple diagonal deep N-well (DDNW) regions forming a diagonal sub-surface mesh structure in accordance with an embodiment of the present invention.

 Figure 5B illustrates a top view of multiple N-wells and multiple diagonal deep
10 N-well (DDNW) regions forming a diagonal sub-surface mesh structure in accordance with an embodiment of the present invention.

 Figure 6A illustrates a top view of multiple diagonal deep N-well (DDNW) regions forming a first diagonal sub-surface strip structure in accordance with an
15 embodiment of the present invention.

 Figure 6B illustrates a top view of multiple diagonal deep N-well (DDNW) regions forming a second diagonal sub-surface strip structure in accordance with an
embodiment of the present invention.

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 Figure 7 illustrates a top view of multiple axial deep N-well (ADNW) regions forming an axial sub-surface mesh structure in accordance with an embodiment of the present invention.

Figure 8A illustrates a top view of multiple axial deep N-well (ADNW) regions forming a first axial sub-surface strip structure in accordance with an embodiment of the present invention.

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Figure 8B illustrates a top view of multiple axial deep N-well (ADNW) regions forming a second axial sub-surface strip structure in accordance with an embodiment of the present invention.

10 Figure 9A illustrates a top view of a semiconductor device, showing a metal mesh structure in accordance with an embodiment of the present invention.

Figure 9B illustrates the relative positioning of metal layers, an N-well region, and a deep N-well region beneath a surface of a semiconductor device in accordance
15 with an embodiment of the present invention.

Figure 10 illustrates a top view of a semiconductor device, showing a metal ring structure in accordance with an embodiment of the present invention.

20 Figure 11 illustrates a top view of a semiconductor device, showing a metal branching tree structure in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference will now be made in detail to embodiments of the present invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with these embodiments, it will be understood that

5 they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of

10 the present invention. However, it will be recognized by one of ordinary skill in the art that the present invention may be practiced without these specific details.

Although the following description of the present invention will focus on routing

15 a body-bias voltage to pFETS (or p-type MOSFETS) formed in surface N-wells via a conductive sub-surface region of N-type doping when a p-type substrate and an N-well process are utilized, the present invention is equally applicable to routing a body-bias voltage to nFETS (or n-type MOSFETS) formed in surface P-wells via a

20 conductive sub-surface region of P-type doping when an n-type substrate and a P-well process are utilized.

LAYOUT PATTERNS FOR DEEP N-WELL REGION TO ROUTE BODY-BIAS VOLTAGE

Figure 1 illustrates a top view of a pFET 50 (or p-type MOSFET) formed in an N-well 10 when a p-type substrate and an N-well process are utilized in accordance with an embodiment of the present invention, whereas the pFET 50 has a body-bias voltage V_{nw} applied to its bulk/body B terminal. As depicted in Figure 1, the pFET 50 has gate G, drain D (p-type doping), source S (p-type doping), and bulk/body B terminals. In particular, the bulk/body B terminal is coupled to the N-well 10. Hence, a voltage applied to the bulk/body B terminal is received by the N-well 10. The N-well has an n-type doping. Regions of a semiconductor device that are doped with an n-type dopant have one type of conductivity while regions that are doped with a p-type dopant have another type of conductivity. Typically, various dopant concentrations are utilized in different regions of the semiconductor device.

The pFET 50 is body-biased to influence its performance. Without body-biasing, the source S and bulk/body B terminals are coupled together. With body-biasing, the source S and bulk/body B terminals are not coupled together. Body-biasing enables controlling the potential difference between the source S and bulk/body B terminals of the pFET 50, providing the ability to electrically tune the threshold voltage level of the pFET 50.

In the case of body-biasing, the bulk/body B terminal receives a body-bias voltage V_{nw} . As described above, the bulk/body B terminal represents a connection to the N-well 10. Thus, the body-bias voltage V_{nw} is applied to the N-well 10.

5 Rather than generating an entire new physical layout for a semiconductor device to support the pFET 50 having the body-bias voltage V_{nw} , an existing physical layout can be modified. In particular, the existing physical layout is modified by including a deep N-well region to route the body-bias voltage V_{nw} to the N-wells 10 which generally are separated by P-well regions, whereas the deep N-well represents
10 a conductive sub-surface well layer that is beneath the surface N-well 10. This avoids the need to create another surface routing layer on a surface of the semiconductor device that does not have much free surface area for additional routing.

 Several layout patterns for the deep N-well region are described herein. These
15 layout patterns facilitate routing the body-bias voltage in the semiconductor device. The layout patterns include a diagonal sub-surface mesh structure (see Figure 5A), an axial sub-surface mesh structure (see Figure 7), a diagonal sub-surface strip structure (see Figure 6A and Figure 6B), and an axial sub-surface strip structure (see Figure 8A and Figure 8B). A particular layout pattern is selected for an area of the semiconductor
20 device according to several factors as will be described below. Once the particular layout pattern is selected, the layout for the deep N-well region can be generated in an automated manner.

The body-bias voltage V_{nw} is routed to the N-wells via one or more deep N-well regions (which are conductive sub-surface well layers) as opposed to surface metal layers. In one embodiment, the deep N-well region is a diagonal deep N-well region as will be described below. In another embodiment, the deep N-well region is an axial deep N-well region as will be described below. The advantage of this approach is that while typically there is little or no room on the densely packed surface area of the semiconductor device for extra metal routing layers, the area beneath the surface of the semiconductor device is often underutilized due to the fact that routing signals through wells is generally prohibited by the poor frequency response and potentially unfavorable resistance of the wells. In the present invention, rather than carrying signals, the deep N-well regions serve to hold and distribute the body-bias voltage V_{nw} .

Figure 2A illustrates the relative positioning of an N-well 10 (also known as a surface N-well) and a deep N-well region 20 beneath a surface 70 of a semiconductor device in accordance with an embodiment of the present invention. The N-well 10 is formed beneath the surface 70 of the semiconductor device and has an N-type doping. The deep N-well region 20 is formed beneath the N-well 10 such that the deep N-well region 20 and the N-well 10 share a sub-surface conductive boundary 25 that allows the deep N-well region 20 to function like a conductive sub-surface routing layer for routing the body-bias voltage V_{nw} to the N-wells. That is, the deep N-well region 20 contacts the N-well 10 along the sub-surface conductive boundary 25. Moreover, the deep N-well region 20 is buried under the surface 70 of the semiconductor device.

The deep N-well region 20 has an N-type doping. It should be understood that if an n-type substrate and a P-well process were utilized, a deep well of P-type doping would be utilized to function as a conductive sub-surface routing layer for routing the body-bias voltage to the surface P-wells.

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The dimensions and size of the sub-surface conductive boundary 25 determine the resistance of the conductive path between the N-well 10 and the deep N-well region 20. As the size of the sub-surface conductive boundary 25 is increased, the resistance of the sub-surface conductive path between the N-well 10 and the deep N-well region 20 is lowered to create a low-resistance conductive path.

Figure 2B illustrates a side view of a deep N-well region coupled to the N-well_1 and the N-well_2 in accordance with an embodiment of the present invention, showing the routing of the body-bias voltage. As illustrated in Figure 2B, there is a first sub-surface conductive boundary 396 between the N-well_1 and the deep N-well region 310. Moreover, there is a second sub-surface conductive boundary 397 between the N-well_2 and the deep N-well region 310. The surface N-well_1 has a PFET 370. Also, the surface N-well_2 has a PFET 370. The P-well region has an NFET 380 and separates the N-well_1 and the N-well_2. The body-bias voltage V_{nw} is routed to the N-well_1 and the N-well_2 via the first and second sub-surface conductive boundaries 396 and 397.

A top view of a first arrangement of the N-well_1 and the N-well_2 in accordance with an embodiment of the present invention is illustrated in Figure 3A. As depicted in Figure 3A, the N-well_1 and the N-well_2 have an axial orientation. That is, the N-well_1 and the N-well_2 are positioned along an axis (e.g., x-axis). The N-well_1 and the N-well_2 have an N-type doping. The body-bias voltage V_{nw} is routed to the N-well_1 and the N-well_2 so that the pFETs 370 can be body-biased via the deep N-well region. Thus, a contact for the body-bias voltage V_{nw} can be formed wherever there is free surface area, such as above the N-well_1, the N-well_2, or deep N-well region. Since the N-well_1 and the N-well_2 are separated by a P-type region or P-well region 385 on which the nFETS 380 are formed, the layout pattern of the deep N-well is carefully selected to avoid isolating the P-type region or P-well region 385 on which the nFETS 380 are formed, allowing the formation of conductive paths between the P-well region 385 and a sub-surface layer (e.g., doped with P-type material) that is formed beneath the deep N-well region. Here, the N-well_1 and the N-well_2 are separated by the length d .

Figure 3B illustrates a top view of a second arrangement of the N-well_3 and the N-well_4 in accordance with an embodiment of the present invention. As depicted in Figure 3B, the N-well_3 and the N-well_4 have an axial orientation. That is, the N-well_3 and the N-well_4 are positioned along an axis (e.g., y-axis). The N-well_3 and the N-well_4 have an N-type doping. The body-bias voltage V_{nw} is routed to the N-well_3 and the N-well_4 so that the pFETs 370 can be body-biased via the deep N-well region. Thus, a contact for the body-bias voltage V_{nw} can be formed wherever

there is free surface area, such as above the N-well_3, the N-well_4, or deep N-well region. Since the N-well_3 and the N-well_4 are separated by a P-type region or P-well region 385 on which the nFETS 380 are formed, the layout pattern of the deep N-well is carefully selected to avoid isolating the P-type region or P-well region 385 on which the nFETS 380 are formed, allowing the formation of conductive paths between the P-well region 385 and a sub-surface layer (e.g., doped with P-type material) that is formed beneath the deep N-well region. Here, the N-well_3 and the N-well_4 are separated by the length m.

Figure 4 illustrates a top view of a semiconductor device 400 in accordance with an embodiment of the present invention, showing multiple areas 401-404 each area corresponding to a separate layout pattern for the deep N-well. In general, the layout distribution of surface N-wells and surface P-type regions or P-wells on the semiconductor device 400 is characterized by particular patterns. The semiconductor device 400 can be divided according to these particular patterns into multiple areas 401-404. Alternatively, the semiconductor device 400 may have a single layout distribution of surface N-wells and surface P-type regions or P-wells.

Once the layout pattern of the surface N-wells and surface P-type regions or P-wells are recognized, a layout pattern for the deep N-well region can be selected for the particular area. The layout patterns for the deep N-well region include a diagonal sub-surface mesh structure (see Figure 5A), an axial sub-surface mesh structure (see Figure 7), a diagonal sub-surface strip structure (see Figure 6A and Figure 6B), and an

axial sub-surface strip structure (see Figure 8A and Figure 8B). The factors evaluated in selecting a particular layout pattern for the deep N-well region include: providing a low resistance conductive path for routing the body-bias voltage and avoiding the isolation of the P-type region or P-well region 385 (Figures 3A and 3B) on which the nFETS 380 are formed to allow the formation of conductive paths between the P-well region 385 and a sub-surface layer (e.g., doped with P-type material) that is formed beneath the deep N-well region.

Moreover, the primary factors in determining which particular layout pattern for the deep N-well region to use is the type of layout pattern (e.g., horizontal strips or vertical strips) of the surface N-wells (see Figures 3A and 3B) and the separation length between adjacent surface N-wells (e.g., separation length d in Figure 3A, and separation length m in Figure 3B). Since each type of layout pattern of the surface N-wells (see Figures 3A and 3B) exhibits unique characteristics, a layout pattern for the deep N-well region is selected that is appropriate for those characteristics exhibited by the layout pattern of the surface N-wells. Within each area 401-404, adjustments to the layout pattern of the deep N-well can be made to overcome any violations of the layout design rules and to improve the factors described above.

Figure 5A illustrates a top view of multiple diagonal deep N-well (DDNW) regions forming a diagonal sub-surface mesh structure 500 in accordance with an embodiment of the present invention. Rather than having a continuous planar layer for the deep N-well, multiple diagonal deep N-well (DDNW) regions are patterned

according to a layout pattern. As depicted in Figure 5A, each diagonal deep N-well region 510A-510E and 512A-512D has a strip shape, is formed beneath the surface N-well layer of a semiconductor device, and is doped with an N-type material. The diagonal deep N-well regions 510A-510E are formed in a first parallel orientation

5 while the diagonal deep N-well regions 512A-512D are formed in a second parallel orientation. The first parallel orientation and the second parallel orientation are orthogonal to each other and are diagonal (or slanted) with respect to the N-well regions of Figures 3A and 3B. In an embodiment, the first parallel orientation and the N-well regions of Figures 3A and 3B form an angle that is approximately 45 degrees.

10 Additionally, in an embodiment, the second parallel orientation and the N-well regions of Figures 3A and 3B form an angle that is approximately 45 degrees. Thus, the diagonal deep N-well regions 510A-510E and 512A-512D form a diagonal sub-surface mesh structure 500 for routing the body-bias voltage V_{nw} to the N-well regions so that the pFETs can be body-biased.

15 As described above with respect to Figures 2A and 2B, the layer corresponding to the deep N-well region is below the layer corresponding to the surface N-well regions. Hence, sub-surface conductive boundaries can be formed between the N-well regions and the diagonal sub-surface mesh structure 500 to provide a plurality of sub-surface conductive paths between N-well regions without isolating the P-well region located between the N-wells. That is, the diagonal sub-surface mesh structure 500 contacts the N-wells along the sub-surface conductive boundaries (e.g., sub-

surface conductive boundary 25 (Figure 2A) and sub-surface conductive boundaries 396 and 397 (Figure 2B).

5 The orientation of the diagonal sub-surface mesh structure 500 is diagonal with respect to the orientation of the N-well regions of Figures 3A and 3B. In an embodiment, the diagonal sub-surface mesh structure 500 is rotated approximately 45 degrees with respect to the N-well regions of Figures 3A and 3B. It should be understood that the diagonal sub-surface mesh structure 500 can have other configurations. For example, the gaps 540A and 540B between adjacent diagonal
10 deep N-well regions can vary in size. Moreover, the ratio of diagonal deep N-well regions to gap area 430 can vary.

Additionally, the diagonal sub-surface mesh structure 500 enables the nFETS (n-type MOSFETS) 380 (Figures 3A and 3B) to be body-biased in any manner by
15 preventing isolation of a P-type region or P-well region 385 (Figure 3A and 3B) on which the nFETS 380 are formed. The gap area 530 between diagonal deep N-well regions 510A-510E and 512A-512D prevent isolation of the P-well region 385 and enable a conductive path between the P-well region 385 and a sub-surface layer that is beneath the diagonal deep N-well regions 510A-510E and 512A-512D. In an
20 embodiment, the area of the diagonal sub-surface mesh structure 500 is equally divided between diagonal deep N-well regions (e.g., 510A-510E and 512A-512D) and gap area 530.

As discussed above, a contact for the body-bias voltage V_{nw} can be formed wherever there is free space, such as above the N-well regions or above the diagonal deep N-well regions 510A-510E and 512A-512D. Moreover, the location and size of the diagonal sub-surface mesh structure 500 is based on the distribution of the N-wells and the P-type regions or P-wells, whereas the goal is to provide low resistance conductive paths for the body-bias voltage V_{nw} .

However, the size of the diagonal sub-surface mesh structure 500 should avoid isolating the P-type regions or P-wells 385 (Figures 3A and 3B) from sub-surface layers that are formed beneath the diagonal deep N-well regions 510A-510E and 512A-512D. Moreover, the gap area 530 is sized so that to provide a low-resistance conductive path between the P-type regions or P-wells 385 and a sub-surface layer that is formed beneath the diagonal deep N-well regions, whereas the greater the gap area 530 the lower the resistance of this conductive path. Additionally, lateral diffusion and lateral depletion can further reduce the gap area 530, potentially pinching-off this conductive path between the P-type regions or P-wells 385 and a sub-surface layer that is formed beneath the diagonal deep N-well regions. As a solution to this situation, the gaps 540A and 540B between adjacent diagonal deep N-well regions are made sufficiently wide to avoid pinching-off this conductive path between the P-type regions or P-wells 385 and a sub-surface layer that is formed beneath the diagonal deep N-well regions. Yet, as the number and size of the diagonal deep N-well regions are increased, the resistance of the conductive path for routing the body-bias voltage V_{nw} is decreased because there are larger and more sub-surface

conductive boundaries between the N-well regions and the diagonal deep N-well regions. Hence, there is a trade-off between the gap area 530 and the diagonal deep N-well regions in each design situation.

5 Figure 5B illustrates a top view of multiple N-wells (e.g., N-well_1 and the N-well_2) and multiple diagonal deep N-well (DDNW) regions forming a diagonal sub-surface mesh structure in accordance with an embodiment of the present invention. Here, the diagonal deep N-well regions 410A and 410B are orthogonal to the diagonal deep N-well regions 412A, 412B, and 412C. Thus, the diagonal deep N-well
10 regions 412A, 412B, 412C, 410A, and 410B form a diagonal sub-surface mesh structure 490 for routing the body-bias voltage V_{nw} to the N-well_1 and the N-well_2 so that the pFETs 470 can be body-biased. In an embodiment, the area of the diagonal sub-surface mesh structure 490 is equally divided between diagonal deep N-well regions and gap area 430.

15 It should be understood that the diagonal sub-surface mesh structure 490 can have other configurations. The gaps 440A and 440B between adjacent diagonal deep N-well regions can vary in size. Moreover, the ratio of diagonal deep N-well regions to gap area 430 can vary. The regions 495 between diagonal deep N-well regions
20 prevent isolation of the P-well region 485 and enable a conductive path between the P-well region 485 and a sub-surface layer that is beneath the diagonal deep N-well regions 412A, 412B, 412C, 410A, and 410B.

A top view of multiple diagonal deep N-well (DDNW) regions forming a first diagonal sub-surface strip structure 600A in accordance with an embodiment of the present invention is illustrated in Figure 6A. In this layout pattern, each diagonal deep N-well region 610A-610D has a strip shape, is formed beneath the surface N-well layer of a semiconductor device, and is doped with an N-type material. The diagonal deep N-well regions 610A-610D are formed in a first parallel orientation. The first parallel orientation is diagonal (or slanted) with respect to the surface N-well regions (e.g., N-well_A, N-well_B, and N-well_C). In an embodiment, the first parallel orientation and the N-well regions form an angle that is approximately 45 degrees. In this case, the combination of the surface N-well regions (e.g., N-well_A, N-well_B, and N-well_C) and the first diagonal sub-surface strip structure 600A forms a mesh-type arrangement for routing the body-bias voltage to the surface N-well regions so that the pFETs can be body-biased.

As described above with respect to Figures 2A and 2B, the layer corresponding to the deep N-well region is below the layer corresponding to the surface N-well regions. Hence, sub-surface conductive boundaries can be formed between the N-well regions and the first diagonal sub-surface strip structure 600A to provide a plurality of sub-surface conductive paths between N-well regions without isolating the P-well region located between the N-wells. That is, the first diagonal sub-surface strip structure 600A contacts the N-wells along the sub-surface conductive boundaries (e.g., sub-surface conductive boundary 25 (Figure 2A) and sub-surface conductive boundaries 396 and 397 (Figure 2B)).

As described above, the combination of the surface N-well regions (e.g., N-well_A, N-well_B, and N-well_C) and diagonal deep N-well regions 610A-610D, which form the first diagonal sub-surface strip structure 600A, facilitate the routing of the body-bias voltage V_{nw} to the N-well regions so that the pFETs can be body-biased. The first diagonal sub-surface strip structure 600A can be utilized in areas of the semiconductor device that have a dense layout such as areas corresponding to a SRAM (static random access memory). It should be understood that the first diagonal sub-surface strip structure 600A can have other configurations. The gap 640A between adjacent diagonal deep N-well regions can vary in size. Moreover, the ratio of diagonal deep N-well regions to gap area 630 can vary.

Figure 6B illustrates a top view of multiple diagonal deep N-well (DDNW) regions forming a second diagonal sub-surface strip structure 600B in accordance with an embodiment of the present invention. In this layout pattern, each diagonal deep N-well region 612A-612D has a strip shape, is formed beneath the surface N-well layer of a semiconductor device, and is doped with an N-type material. The diagonal deep N-well regions 612A-612D are formed in a second parallel orientation. The second parallel orientation is diagonal (or slanted) with respect to the surface N-well regions (e.g., N-well_D, N-well_E, and N-well_F). In an embodiment, the second parallel orientation and the N-well regions form an angle that is approximately 45 degrees. In this case, the combination of the surface N-well regions (e.g., N-well_D, N-well_E, and N-well_F) and the second diagonal sub-surface strip structure 600B

forms a mesh-type arrangement for routing the body-bias voltage to the surface N-well regions so that the pFETs can be body-biased.

As described above with respect to Figures 2A and 2B, the layer corresponding to the deep N-well region is below the layer corresponding to the surface N-well regions. Hence, sub-surface conductive boundaries can be formed between the N-well regions and the second diagonal sub-surface strip structure 600B to provide a plurality of sub-surface conductive paths between N-well regions without isolating the P-well region located between the N-wells. That is, the second diagonal sub-surface strip structure 600B contacts the N-wells along the sub-surface conductive boundaries (e.g., sub-surface conductive boundary 25 (Figure 2A) and sub-surface conductive boundaries 396 and 397 (Figure 2B).

As described above, the combination of the surface N-well regions (e.g., N-well_D, N-well_E, and N-well_F) and diagonal deep N-well regions 612A-612D, which form the second diagonal sub-surface strip structure 600B, facilitate routing of the body-bias voltage V_{nw} to the N-well regions so that the pFETs can be body-biased. The second diagonal sub-surface strip structure 600B can be utilized in areas of the semiconductor device that have a dense layout such as areas corresponding to a SRAM (static random access memory). It should be understood that the second diagonal sub-surface strip structure 600B can have other configurations. The gap 640B between adjacent diagonal deep N-well regions can vary in size. Moreover, the ratio of diagonal deep N-well regions to gap area 630 can vary.

Figure 7 illustrates a top view of multiple axial deep N-well (ADNW) regions forming an axial sub-surface mesh structure 700 in accordance with an embodiment of the present invention. As depicted in Figure 7, each axial deep N-well region 710A-710E and 712A-712D has a strip shape, is formed beneath the surface N-well layer of a semiconductor device, and is doped with an N-type material. The axial deep N-well regions 710A-710E are formed in a first parallel orientation while the diagonal deep N-well regions 712A-712D are formed in a second parallel orientation. The first parallel orientation and the second parallel orientation are orthogonal to each other and are axially positioned with respect to the N-well regions of Figures 3A and 3B. That is, the first parallel orientation and the second parallel orientation are oriented along an axis (e.g., y-axis or x-axis) in the same manner as the N-well regions of Figures 3A and 3B. In an embodiment, the first parallel orientation is parallel to the N-well regions of Figure 3A and is perpendicular to the N-well regions of Figure 3B. Additionally, in an embodiment, the second parallel orientation is parallel to the N-well regions of Figure 3B and is perpendicular to the N-well regions of Figure 3A. Thus, the axial deep N-well regions 710A-710E and 712A-712D form an axial sub-surface mesh structure 700 for routing the body-bias voltage V_{nw} to the N-well regions so that the pFETs can be body-biased.

As described above with respect to Figures 2A and 2B, the layer corresponding to the deep N-well region is below the layer corresponding to the surface N-well regions. Hence, sub-surface conductive boundaries can be formed between the N-

well regions and the axial sub-surface mesh structure 700 to provide a plurality of sub-surface conductive paths between N-well regions without isolating the P-well region located between the N-wells. That is, the axial sub-surface mesh structure 700 contacts the N-wells along the sub-surface conductive boundaries (e.g., sub-surface conductive boundary 25 (Figure 2A) and sub-surface conductive boundaries 396 and 397 (Figure 2B).

It should be understood that the axial sub-surface mesh structure 700 can have other configurations. For example, the gaps 740A and 740B between adjacent axial deep N-well regions can vary in size. Moreover, the ratio of axial deep N-well regions to gap area 730 can vary.

Additionally, the axial sub-surface mesh structure 700 enables the nFETS (n-type MOSFETS) 380 (Figures 3A and 3B) to be body-biased in any manner by preventing isolation of a P-type region or P-well region 385 (Figure 3A and 3B) on which the nFETS 380 are formed. The gap area 730 between axial deep N-well regions 710A-710E and 712A-712D prevent isolation of the P-well region 385 and enable a conductive path between the P-well region 385 and a sub-surface layer that is beneath the axial deep N-well regions 710A-710E and 712A-712D. In an embodiment, the area of the axial sub-surface mesh structure 700 is equally divided between axial deep N-well regions (e.g., 710A-710E and 712A-712D) and gap area 730.

As discussed above, a contact for the body-bias voltage V_{nw} can be formed wherever there is free space, such as above the N-well regions or above the axial deep N-well regions 710A-710E and 712A-712D. Moreover, the location and size of the axial sub-surface mesh structure 700 is based on the distribution of the N-wells and the P-type regions or P-wells, whereas the goal is to provide low resistance conductive paths for the body-bias voltage V_{nw} .

As described above, the size of the axial sub-surface mesh structure 700 should avoid isolating the P-type regions or P-wells 385 (Figures 3A and 3B) from sub-surface layers that are formed beneath the axial deep N-well regions 710A-710E and 712A-712D. Moreover, the gap area 730 is sized so that to provide a low-resistance conductive path between the P-type regions or P-wells 385 and a sub-surface layer that is formed beneath the axial deep N-well regions, whereas the greater the gap area 730 the lower the resistance of this conductive path. Additionally, lateral diffusion and lateral depletion can further reduce the gap area 730, potentially pinching-off this conductive path between the P-type regions or P-wells 385 and a sub-surface layer that is formed beneath the axial deep N-well regions. As a solution to this situation, the gaps 740A and 740B between adjacent axial deep N-well regions are made sufficiently wide to avoid pinching-off this conductive path between the P-type regions or P-wells 385 and a sub-surface layer that is formed beneath the axial deep N-well regions. Yet, as the number and size of the axial deep N-well regions are increased, the resistance of the conductive path for routing the body-bias voltage V_{nw} is decreased because there are larger and more sub-surface conductive boundaries

between the N-well regions and the axial deep N-well regions. Hence, there is a trade-off between the gap area 730 and the axial deep N-well regions in each design situation.

5 Figure 8A illustrates a top view of multiple axial deep N-well (ADNW) regions forming a first axial sub-surface strip structure 800A in accordance with an embodiment of the present invention. In this layout pattern, each axial deep N-well region 810A-810D has a strip shape, is formed beneath the surface N-well layer of a semiconductor device, and is doped with an N-type material. The axial deep N-well
10 regions 810A-810D are formed in a first parallel orientation. The first parallel orientation is parallel to the surface N-well regions (e.g., N-well_G, N-well_H, and N-well_I). In this case, the combination of the surface N-well regions (e.g., N-well_G, N-well_H, and N-well_I) and the first axial sub-surface strip structure 800A forms a mesh-type arrangement for routing the body-bias voltage to the surface N-well regions
15 so that the pFETs can be body-biased.

As described above with respect to Figures 2A and 2B, the layer corresponding to the deep N-well region is below the layer corresponding to the surface N-well regions. Hence, sub-surface conductive boundaries can be formed between the N-
20 well regions and the first axial sub-surface strip structure 800A to provide a plurality of sub-surface conductive paths between N-well regions without isolating the P-well region located between the N-wells. That is, the first axial sub-surface strip structure 800A contacts the N-wells along the sub-surface conductive boundaries (e.g., sub-

surface conductive boundary 25 (Figure 2A) and sub-surface conductive boundaries 396 and 397 (Figure 2B).

As described above, the combination of the surface N-well regions (e.g., N-well_G, N-well_H, and N-well_I), and the axial deep N-well regions 810A-810D, which form the first axial sub-surface strip structure 800A, facilitate routing of the body-bias voltage V_{nw} to the N-well regions so that the pFETs can be body-biased. The first axial sub-surface strip structure 800A can be utilized in areas of the semiconductor device that have a dense layout and are oriented according to the N-well regions of Figure 3B. It should be understood that the first axial sub-surface strip structure 800A can have other configurations. The gap 840A between adjacent axial deep N-well regions can vary in size. Moreover, the ratio of axial deep N-well regions to gap area 830 can vary.

Figure 8B illustrates a top view of multiple axial deep N-well (ADNW) regions forming a second axial sub-surface strip structure 800B in accordance with an embodiment of the present invention. In this layout pattern, each axial deep N-well region 812A-812D has a strip shape, is formed beneath the surface N-well layer of a semiconductor device, and is doped with an N-type material. The axial deep N-well regions 812A-812D are formed in a second parallel orientation. The second parallel orientation is parallel to the surface N-well regions (e.g., N-well_J, N-well_K, and N-well_L). In this case, the combination of the surface N-well regions (e.g., N-well_J, N-well_K, and N-well_L) and the second axial sub-surface strip structure 800B forms a

mesh-type arrangement for routing the body-bias voltage to the surface N-well regions so that the pFETs can be body-biased.

As described above with respect to Figures 2A and 2B, the layer corresponding to the deep N-well region is below the layer corresponding to the surface N-well regions. Hence, sub-surface conductive boundaries can be formed between the N-well regions and the second axial sub-surface strip structure 800B to provide a plurality of sub-surface conductive paths between N-well regions without isolating the P-well region located between the N-wells. That is, the second axial sub-surface strip structure 800B contacts the N-wells along the sub-surface conductive boundaries (e.g., sub-surface conductive boundary 25 (Figure 2A) and sub-surface conductive boundaries 396 and 397 (Figure 2B)).

As described above, the combination of the surface N-well regions (e.g., N-well_J, N-well_K, and N-well_L), and the axial deep N-well regions 812A-812D, which form the second axial sub-surface strip structure 800A, facilitate routing of the body-bias voltage V_{nw} to the N-well regions so that the pFETs can be body-biased. The second axial sub-surface strip structure 800B can be utilized in areas of the semiconductor device that have a dense layout and are oriented according to the N-well regions of Figure 3A. It should be understood that the second axial sub-surface strip structure 800B can have other configurations. The gap 840B between adjacent axial deep N-well regions can vary in size. Moreover, the ratio of axial deep N-well regions to gap area 830 can vary.

ROUTING BODY-BIAS VOLTAGE WITH A LOW RC STRUCTURE COMPRISED OF A DEEP N-WELL STRUCTURE COUPLED TO A METAL STRUCTURE

5 A noted above, the following description of the present invention is equally applicable to a p-type substrate and an N-well process, as well as to an n-type substrate and a P-well process.

 As described above, the deep N-well region can have many different layout
10 patterns for routing the body-bias voltage. Examples of these layout patterns include a diagonal sub-surface mesh structure (Figures 5A and 5B), an axial sub-surface mesh structure (Figure 7), a diagonal sub-surface strip structure (Figures 6A and 6B), and an axial sub-surface strip structure (Figures 8A and 8B).

15 One negative aspect of using the deep N-well region to route the body-bias voltage concerns the RC property of the deep N-well structures described above. The RC property of these deep N-well structures tends to be high, increasing the time necessary to change the body-bias voltage coupled to these deep N-well structures.

20 Although the discussion below will focus on the RC property of the deep N-well mesh structures (e.g., diagonal sub-surface mesh structure (Figures 5A and 5B) and axial sub-surface mesh structure (Figure 7)), the discussion is equally applicable to other deep N-well structures utilized to route the body-bias voltage.

The deep N-well mesh structures (e.g., diagonal sub-surface mesh structure (Figures 5A and 5B) and axial sub-surface mesh structure (Figure 7)) have a substantial RC property. This high RC property leads to delay in charging and
5 discharging the deep N-well mesh structures.

The values provided henceforth to calculate this RC property are illustrative. The present invention is not limited to these values. The values may be different in other cases for numerous reasons (e.g., manufacturing process utilized, materials
10 utilized, etc.). The sheet resistance of the deep N-well region is approximately 1000 ohms per square. The sheet resistance of the deep N-well mesh structures (e.g., diagonal sub-surface mesh structure (Figures 5A and 5B) and axial sub-surface mesh structure (Figure 7)) is approximately 2000 ohms per square, which represents "R" of RC. Moreover, the capacitance of the deep N-well mesh structures is approximately
15 50 nF/cm² which represents "C" of RC, whereas nF indicates nanofarads and cm indicates centimeters. In a 1 cm² chip die, the distributed RC of a deep N-well mesh structure is calculated as follows:

$$\text{distributed RC} = RC/2 = [(2000 \text{ ohms}) \times (50 \text{ nF})]/2 = 50 \mu\text{s},$$

20 whereas μs represents microseconds. This calculation indicates that the deep N-well mesh structure would experience a delay of at least 50 μs in changing DC voltage levels when supplied with voltage from one edge. Given that semiconductor devices

such as processors are operating at speeds of approximately 1 GHz, 50 μ s is 50,000 processor cycles, whereas GHz represents gigahertz. Hence, a new bias voltage can only be distributed to the transistors every 50,000 processor cycles. If the deep N-well mesh structure changes its DC voltage value in a faster time than 50 μ s, the processor can adjust bias faster. Faster change allows better utilization of body bias advantages.

In an embodiment of the present invention, the RC property is decreased by coupling the deep N-well mesh structure to a metal structure. In one configuration, the metal structure is a metal mesh structure (Figure 9A). In another configuration, the metal structure is a metal ring structure (Figure 10). In yet another configuration, the metal structure is a metal branching tree structure (Figure 11). It should be understood that the metal structure can incorporate one or more of these configurations (e.g., metal mesh structure, metal ring structure, and metal branching tree structure). Moreover, the discussion below will show that the size of the metal utilized in the metal structure is sufficiently small to be implemented by reasonably modifying existing physical layouts.

Figure 9A illustrates a top view of a semiconductor device 900, showing a metal mesh structure 950 in accordance with an embodiment of the present invention. As depicted in Figure 9A, the metal mesh structure 950 has a coarse characteristic. That is, there is a large pitch between the metal wires that form the metal mesh structure 950. The metal mesh structure 950 is coupled to a bias source 970, which provides the body-bias voltage that is routed. Moreover, the metal mesh structure 950 includes

a plurality of spaced tap contacts 960, whereas the tap contacts 960 couple the metal mesh structure 950 to the deep N-well mesh structure (e.g., diagonal sub-surface mesh structure (Figures 5A and 5B) and axial sub-surface mesh structure (Figure 7)). Hence, a combined mesh structure is formed by the metal mesh structure 950 and the deep N-well mesh structure (e.g., diagonal sub-surface mesh structure (Figures 5A and 5B) and axial sub-surface mesh structure (Figure 7)). As will be discussed below, the combined mesh structure has a lower RC property than the RC property of the deep N-well mesh structure. Additionally, this improvement in the RC property does not introduce a noise problem with respect to the body-bias voltage.

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The metal mesh structure 950 can be comprised of a single metal layer. Alternatively, the metal mesh structure 950 can be comprised of multiple metal layers coupled using vias. Moreover, the semiconductor device 900 can have multiple metal mesh structures 950, whereas each metal mesh structure 950 routes a separate body-bias voltage in conjunction with separate portions of the deep N-well mesh structure.

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Figure 9B illustrates the relative positioning of metal layers 91-93, an N-well region 10 (also known as a surface N-well), and a deep N-well region 20 beneath a surface 70 of a semiconductor device in accordance with an embodiment of the present invention. The N-well 10 is formed beneath the surface 70 of the semiconductor device and has an N-type doping. The deep N-well region 20 is formed beneath the N-well 10 such that the deep N-well region 20 and the N-well 10 share a sub-surface conductive boundary 25 that allows the deep N-well region 20 to

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function like a conductive sub-surface routing layer for routing the body-bias voltage V_{nw} to the N-wells. That is, the deep N-well region 20 contacts the N-well 10 along the sub-surface conductive boundary 25. Moreover, the deep N-well region 20 is buried under the surface 70 of the semiconductor device. The deep N-well region 20 has an N-type doping. It should be understood that if an n-type substrate and a P-well process were utilized, a deep well of P-type doping would be utilized to function as a conductive sub-surface routing layer for routing the body-bias voltage to the surface P-wells.

The dimensions and size of the sub-surface conductive boundary 25 determine the resistance of the conductive path between the N-well 10 and the deep N-well region 20. As the size of the sub-surface conductive boundary 25 is increased, the resistance of the sub-surface conductive path between the N-well 10 and the deep N-well region 20 is lowered to create a low-resistance conductive path.

Moreover, one or more layers 75 (e.g., a polysilicon layer, silicon dioxide layer, etc.) are formed above the surface 70. Additionally, a plurality of metal layers 91-93 as formed above the surface 70 and above the layers 75. Typically, the metal layers 91-93 are separated by an interlayer dielectric (ILD) 81-82.

In Figure 9B, there is a tap contact 90 (or tap contact 960 of Figure 9A) from metal layer 91 to the deep N-well region 20. In an embodiment, the tap contact 90 includes a tap contact region 89 that is N⁺ doped, whereas the tap contact region 89 is

surrounded by a N-well 11 that contacts the deep N-well region 20. The deep N-well region 20 and the N-well 11 share a sub-surface conductive boundary 25 that facilitates coupling the metal layer 91 of a metal mesh structure to the deep N-well region 20.

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Referring again to Figure 9A, the metal mesh structure 950 is comprised of metal wires. The values provided henceforth to calculate the RC property of the combined mesh structure formed by the metal mesh structure 950 and the deep N-well mesh structure (e.g., diagonal sub-surface mesh structure (Figures 5A and 5B) and axial sub-surface mesh structure (Figure 7)) are illustrative. The present invention is not limited to these values.

Ideally, the metal wires of the metal mesh structure 950 are made narrow and are spaced apart. Moreover, the placement of the numerous tap contacts 960 to the deep N-well mesh structure involves a tradeoff of at least two objectives. A first objective is to maintain the capacitance of the metal mesh structure 950 relatively small compared to the capacitance of the deep N-well mesh structure, leading to good noise characteristics on the body-bias voltage. A second objective is to provide a sufficient number of tap contacts 960 so that the RC property (or local RC) of the deep N-well mesh structure is lowered due to the presence of closely spaced tap contacts 960. Thus, as the number of tap contacts 960 is increased the local RC of the deep N-well mesh structure is made smaller. However, as the local RC of the deep N-well mesh structure becomes smaller (which may indicate that C is being lowered), the first

objective may be compromised because the capacitance of the metal mesh structure 950 may not be relatively small compared to the capacitance of the deep N-well mesh structure.

5 Following these guidelines for Figure 9A, the metal wire of the metal mesh structure 950 is approximately 1 μm wide, whereas μm represents micrometers. Moreover, each metal wire is placed approximately every 100 μm , whereas μm represents micrometers. Additionally, the tap contacts 960 to the deep N-well mesh structure are created at approximately 100 μm intervals, whereas μm represents
10 micrometers. The sheet resistance of a metal plane is approximately 0.2 ohms per square. However, the sheet resistance of the metal mesh structure 950 is approximately 20 ohms per square (0.2×100), since metal wire (of approximately 1 μm width) is placed approximately every 100 μm . The capacitance of a metal plane is approximately 5 nF/cm^2 , whereas nF indicates nanofarads and cm indicates
15 centimeters. However, the capacitance of the metal mesh structure 950 is approximately 0.1 $\text{nF}/\text{cm}^2 \{[(2) \times (5)]/100\}$, since metal wire (of approximately 1 μm width) is placed approximately every 100 μm , one set horizontal and a second set vertical.

20 As described above, the sheet resistance of the deep N-well region is approximately 1000 ohms per square. The sheet resistance of the deep N-well mesh structures (e.g., diagonal sub-surface mesh structure (Figures 5A and 5B) and axial

sub-surface mesh structure (Figure 7)) is approximately 2000 ohms per square.

Moreover, the capacitance of the deep N-well mesh structures is approximately 50 nF/cm², whereas nF indicates nanofarads and cm indicates centimeters.

5 Assuming a 1 cm² chip die, the combined mesh structure formed by the metal mesh structure 950 and the deep N-well mesh structure (e.g., diagonal sub-surface mesh structure (Figures 5A and 5B) and axial sub-surface mesh structure (Figure 7)) has improved characteristics relative to the characteristics of the deep N-well mesh structure. The sheet resistance (or "R" of RC) of the combined mesh structure is
10 dominated by the metal mesh structure 950 (approximately 20 ohms per square) rather than the deep N-well mesh structure (approximately 2000 ohms per square). Additionally, the capacitance (or "C" of RC) of the combined mesh structure is dominated by the deep N-well mesh structure (approximately 50 nF/cm²) rather than the metal mesh structure 950 (approximately 0.1 nF/cm²). Hence, the distributed RC of
15 a combined mesh structure is calculated as follows:

$$\text{distributed RC} = RC/2 = [(20 \text{ ohms}) \times (50 \text{ nF})]/2 = 0.5 \mu\text{s},$$

whereas μs represents microseconds. This calculation indicates that the combined
20 mesh structure would experience a delay of at least 0.5 μs in changing DC voltage levels, whereas 0.5 μs is 100 times better than 50 μs as calculated above for the deep N-well mesh structure. If semiconductor devices such as processors are operating at

speeds of approximately 1 GHz, 0.5 μ s is 500 processor cycles, whereas GHz represents gigahertz. Hence, the combined mesh structure would allow faster changes in bias voltage, and better utilization of body bias advantages.

5 Moreover, the local RC of the deep N-well mesh structure becomes smaller, even negligible. This occurs because RC is a function of a length value of the distributed R and C. In particular, RC is proportional to the square of this length value. Since the tap contacts 960 to the deep N-well mesh structure are created at approximately 100 μ m intervals, the length value is reduced from approximately 1 cm
10 to approximately 100 μ m. Hence, the local RC of the deep N-well mesh structure is reduced and improved by a factor of 100^2 (or $1\text{cm}/100\mu\text{m})^2$, which is 10000. In particular, the local RC=50us of the deep N-well mesh structure becomes local RC=5ns, whereas μ s represent microseconds and ns represents nanoseconds.

15 Furthermore, the metal mesh structure 950 adds approximately 0.2% capacitance (C = approximately 0.1 nF/cm²) to the deep N-well mesh structure (C = approximately 50 nF/cm²). This indicates capacitance coupled noise on the metal mesh structure 950 can increase body-bias voltage noise by no more than approximately 0.2%.

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 Additionally, small parasitic currents (on the order of 1 milliamp) can produce significant voltage drops in a deep N-well mesh structure (1 milliamp x 2000 ohms per

square = 2 volts). The coarse characteristic (or large pitch between the metal wires) of the metal mesh structure 950 decreases the effective sheet resistance to approximately 20 ohms per square (1 milliamp x 20 ohms per square = 20 millivolts). Hence, the voltage drop due to parasitic currents can be reduced from 2 volts to 20
5 millivolts.

These calculations demonstrate that a minimal amount of metal can be utilized to provide an improvement in the RC property of the deep N-well mesh structure.

Other choices are possible for the metal mesh structure 950. In general the
10 parameters should be chosen to lower the effective resistance (to improve RC) while adding a small amount of capacitance (to avoid voltage noise).

Also, other choices are possible for the metal structure topology. Examples of other metal structure topologies include the metal ring structure (Figure 10) and the
15 metal branching tree structure (Figure 11). Combinations and permutations of these disclosed metal structure topologies are possible.

Figure 10 illustrates a top view of a semiconductor device 1000, showing a metal ring structure 1060 in accordance with an embodiment of the present invention.
20 As depicted in Figure 10, the metal ring structure 1050 has a ring shape and can have ring configurations other than what is shown. It should be understood that the semiconductor device 1000 can have more than one metal ring structure 1050. The

metal ring structure 1050 is coupled to a bias source 1070, which provides the body-bias voltage that is routed.

Moreover, the metal ring structure 1050 includes a plurality of spaced tap
5 contacts 1060, whereas the tap contacts 1060 couple the metal ring structure 1050 to the deep N-well mesh structure (e.g., diagonal sub-surface mesh structure (Figures 5A and 5B) and axial sub-surface mesh structure (Figure 7)). Hence, a combined structure is formed by the metal ring structure 1050 and the deep N-well mesh structure (e.g., diagonal sub-surface mesh structure (Figures 5A and 5B) and axial
10 sub-surface mesh structure (Figure 7)). The combined structure has a lower RC property than the RC property of the deep N-well mesh structure. Additionally, this improvement in the RC property does not introduce a noise problem with respect to the body-bias voltage. Moreover, the above discussion with respect to the benefits and design choices of the metal mesh structure 950 of Figure 9A is applicable to Figure 10.

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Figure 11 illustrates a top view of a semiconductor device 1100, showing a metal branching tree structure 1150 in accordance with an embodiment of the present invention. As depicted in Figure 11, the metal branching tree structure 1150 has a branching tree shape and can have branching tree configurations other than what is
20 shown. It should be understood that the semiconductor device 1100 can have more than one metal branching tree structure 1150. The metal branching tree structure 1150 is coupled to a bias source 1170, which provides the body-bias voltage that is routed.

Moreover, the metal branching tree structure 1150 includes a plurality of spaced tap contacts 1060, whereas the tap contacts 1160 couple the metal branching tree structure 1150 to the deep N-well mesh structure (e.g., diagonal sub-surface mesh structure (Figures 5A and 5B) and axial sub-surface mesh structure (Figure 7)).

Hence, a combined structure is formed by the metal branching tree structure 1150 and the deep N-well mesh structure (e.g., diagonal sub-surface mesh structure (Figures 5A and 5B) and axial sub-surface mesh structure (Figure 7)). The combined structure has a lower RC property than the RC property of the deep N-well mesh structure.

Additionally, this improvement in the RC property does not introduce a noise problem with respect to the body-bias voltage. Moreover, the above discussion with respect to the benefits and design choices of the metal mesh structure 950 of Figure 9A is applicable to Figure 11.

The above discussion focused on the RC property of the deep N-well mesh structures (e.g., diagonal sub-surface mesh structure (Figures 5A and 5B) and axial sub-surface mesh structure (Figure 7)). However, the above discussion is equally applicable to other deep N-well structures utilized to route the body-bias voltage.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and many modifications and variations are possible in light of the above teaching. The

embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be

5 defined by the Claims appended hereto and their equivalents.